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Design & Implementation of 3-Bit High Speed Flash ADC for Wireless LAN Applications

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Abstract: Analog-to-digital (ADC) converter has become a very important part of electronics in the current digital world as they have a wide variety of applications. Among all the ADC's available, the Flash ADC is one of the fastest ADC but a main drawback of this ADC is its power consumption. So, the main objective of this paper is to implement a high speed low power Flash ADC. A design with 3-bit resolution has been implemented using seven OTA based comparators with a reference voltage of 250mV and a high speed encoder have been implemented using four full adders upon which the integration of different block ADC has been designed. All the circuits are simulated using 180nm technology in Cadence Virtuoso Design environment. The supply voltage is 1.8v.Analog output of each comparator depending upon the comparison between the input and the reference voltage is fed to the encoder and finally the compressed digital output is obtained.

Keywords: Flash ADC, Comparator, OTA, Thermometer to Binary encoder, CMOS 180 nm Technology.

I. INTRODUCTION

With the advancement of technology, digital signal processing has progressed dramatically in recent years. Signal processing in digital domain provides high level of accuracy, low power consumption and small silicon area besides providing flexibility in design and programmability. The design process is also quite faster and cost effective. Furthermore, their implementation makes them suitable for integration with complex digital signal processing blocks in a compatible low-cost technology, particularly CMOS. In the end, it leads us to design a very high speed as well as systems with small die area called System on a chip (SoC), with a smaller number of chips using increased integration level.
This has resulted in the requirement of smart converters between analog and digital signals to cope up with the evolution of technology. Recent in many wireless mobile applications demand very high speed data converters with wide bandwidth, higher signal to noise ratio and variable (adaptive) resolution with optimized power and cost effectiveness. So there is a need for upgrading the performance of data converters to meet the demands of emerging technologies. So it is a challenging issue in the mixed signal design to have high speed, variable resolution data converters with less space and low power consumption.

Digital signal processing has been proved to be a robust and cost effective way of signal processing. In many applications the input and output signals of the system are inherently analog, so a conversion between analog and digital is needed at the interfaces [4]. A/D converter implements the interface between the real word analog signal and the DSP function block [7]. The examples of applications of A/D converters are video-imaging systems, personal communication systems. Higher resolution and higher speed A/D converter is required for applications, such as wireless communication, image processing etc.

II. RELATED WORK

A survey on flash ADC based on certain parameters like reference voltage, supply voltage resolution, Signal to Noise ratio and power consumption has been carried out. Descriptions of some papers are described below.

- Dhrubajyoti&Sagar introduced a Low Power type ADC (Analog-to-Digital Converter) where the conventional comparators have been replaced with the CMOS inverter based comparator designs. The reported structure of the ADC is designed using 180nm technology and it consumes 130.9 µWatt of average power while operating with an input frequency of 30MHz, and a supply voltage of 1.8 Volt. Moreover, with the aim of increasing the design efficiency, an optimized analog layout, which occupies an area of 0.068mm^2, has been presented.[6]

- AditiKar and Alaktold about an area efficient low power high Speed 3-bit Flash Type ADC using bit referenced encoder is proposed in 180 nm CMOS technology. The concept of Threshold Modified Comparator Circuit (TMCC) is also introduced as a modification of the conventional comparator. The proposed design of the ADC occupies an active area of 0.0036 mm2 and consumes 43.146 µW of Average Power while operating with an input frequency (fin) of 10 MHz and a supply voltage of 1.8 Volt.[3]

- Pradeep and Amit give the description of the the design and implementation of a Low Power 3-bit flash Analog to Digital converter (ADC). It includes 7

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comparators and one thermometer to binary encoder. It is implemented in 0.18um CMOS Technology. The pre-simulation of ADC is done in T-Spice. The response time of the comparator equal to 6.82ns and for Flash ADC as 18.77ns.The Simulated result shows the power consumption in Flash ADC as is 36.273mw .The chip area is for Flash ADC is 1044um2.[16]

The prime focus of my work is to develop a high speed flash ADC used in applications of Wireless LAN systems. The main aim of this paper is to implement of a high speed ADC used for the application by Integrating resistor ladder, comparators and thermometer to binary code encoder, flash ADC is designed. All the parameters of ADCs are tested and tradeoff between speed and power is made. A detailed analysis of the implementation is done and compared the proposed ADC with other types of ADCs used for the specific application. The complete ADC is designed and implemented using CMOS 180 nm technology using CADENCE Virtuoso Design environment.

III.FLASH ADC

For high speed applications, flash ADC is often used. Flash ADC is very fast and used for low resolution application due to its parallel architecture. It is best and less complex up to 8 bits. But when the number of bits increased complexity increases since the number of comparator needed is large. The main significance of flash ADC is that they are used within pipeline and sigma delta converters.

Comparators are the key analog building block of any flash ADC and strongly influence performance. A high degree of comparator accuracy is essential for good ADC performance. However, integration of analog circuitry in low voltage scale VLSI technologies results in degraded precision due to large device mismatch and limited voltage swing [6]. Analog offset correction techniques are typically used, but these schemes are increasingly difficult to implement in modern CMOS processes. For this reason, the issue of comparator offset is becoming a bottleneck in the design of flash ADCs.

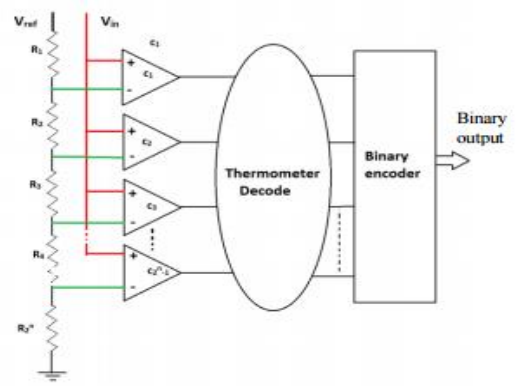

Fig.1Conventional flash ADC

A block diagram of a conventional flash ADC is shown in Fig.1. It has 2^N-1 comparators corresponding to 2^N-1 quantization steps [14]. The total 2^N resistors generate all the reference voltages. The comparator outputs one if the input voltage is larger than the related reference voltage, and vice versa.

The reference voltages are typically generated through the use of a resistor ladder. The thermometer decode block generates a "1 of n" code which is converted to binary.

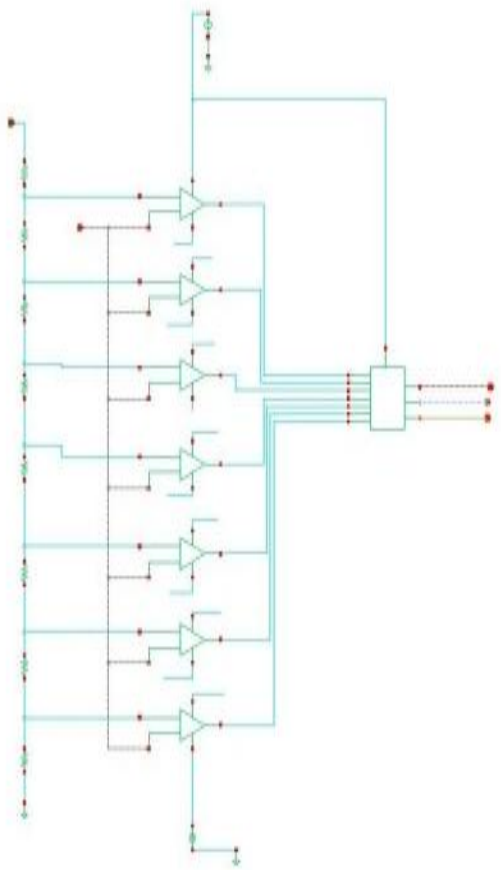

Fig. 2Schematic of Three bit Flash ADC Implementation

As shown in fig. 2 Schematic of Three bit Flash ADC Implementation consists of the three blocks (resistor ladder, 7 comparators and thermometer code to binary code converter) and integrated together to get the functionality of three bit flash ADC. The high speed three bit flash ADC is designed, simulated and verified in CADENCE Design Environment using 180 nm CMOS technology with a power supply of 1.8 V.

IV. DESIGN OF THE COMPARATOR USING OTA

A straightforward approach to make a comparator is to design a high gain amplifier with differential analog input and single-ended large swing output. This kind of comparator is also called open-loop comparators. This comparator consists of the differential input single output OTA connected to an inverter as shown in figure 3.

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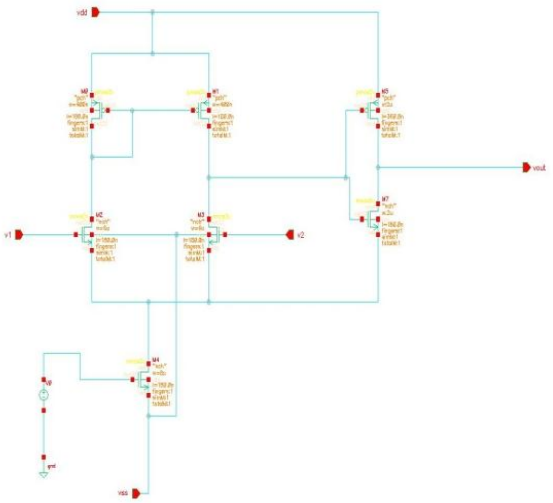

Fig. 3A Comparator circuit Schematic

A. **Transient Analysis**: A sine wave of 10MHz frequency, 500mV p-p is given as input to comparator is shown in fig. 4.When the input is greater than reference the output is HIGH and the output is LOW when input is lesser than the reference.

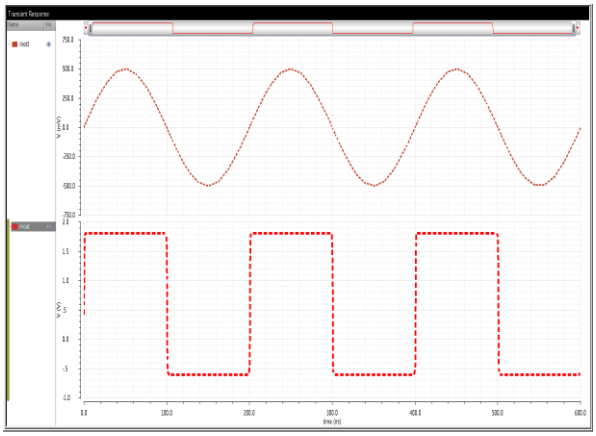

Fig.4 Transient Analysis of a Comparator

The AC response is as shown in the fig. 5. The DC gain of the comparator is 56dB and Unity Gain Bandwidth is 2.5GHz.

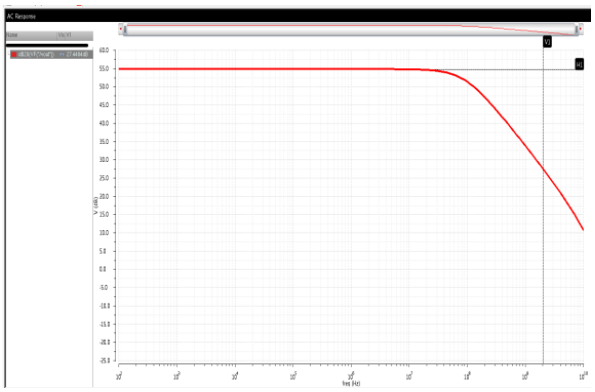

Fig. 5 AC Response of the Comparator

TABLE I PERFORMANCE SUMMARY OF COMPARATOR

Parameter	Proposed Comparator
Technology Size	180nm
Operating Freq.	10 MHz
DC Gain	56 dB
UGB	2.5 GHz

V. ENCODER DESIGN FOR FLASH ADC

Flash ADC comprises of three parts; resistor ladder, comparator and thermometer code to binary code converter. N bit flash ADC architecture requires 2^N-1 comparators for its operation. The reference voltage is generated with the help of 2^N equally sized resistor which constitutes resistor ladder [14]. Since the comparators are working in parallel, flash ADC completes its conversion in one cycle. The output of the comparators is coming in a specific manner which is called thermometer code. The thermometer code is converted into binary code with the help of thermometer code to binary code conversion. The speed of the converter plays a crucial role in the design of flashADC.

Thermometer to Binary encoder is taken as a choice of design which compresses the comparator output having multiple binary inputs into small number of digital output [12]. This encoder depends on the thermometer code which is produced by the array of comparators. It outputs the binary value representing highest position of active input. The logic showing the Thermometer to Binary encoder design for 3 bit output is shown in table 2. The output equation which is obtained using the logic is given below. Using K'map technique below equations are derived-

B0 = T3;
B1 = T1+T3T4+T4T5;
B3 = TOT1+T1T2+T3T4+T5T6.

TABLE II THERMOMETER TO BINARY ENCODER LOGIC TABLE

T0	T1	T2	T3	T4	T5	T6	B0	B1	B2
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

The outputs of comparators form a thermometer code is a combination of a series of zeros and a series of ones, e.g., 000…011…111. Because binary code is usually needed for digital signal processing, a thermometer code is then transformed to a binary code through a (2k-1)-to-k

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Thermometer to Binary encoder, where k is the resolution (bits) of ADCs.

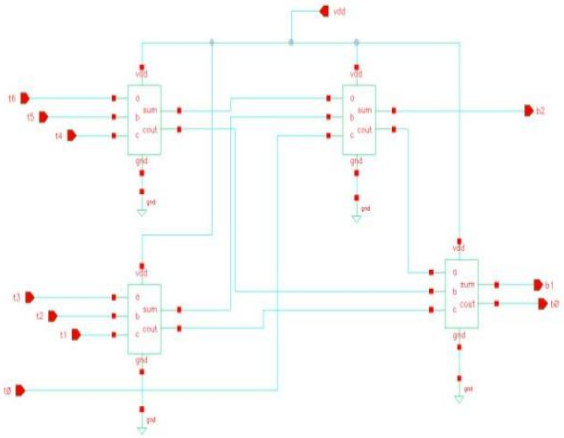

Fig. 6 Thermometer to Binary Encoder

The circuit of the Thermometer to Binary Encoder is shown in Fig. 6. The circuit is simplified to four full adders are connected as shown in the Fig above. The full adders are designed using half adders to simplify the circuit further.

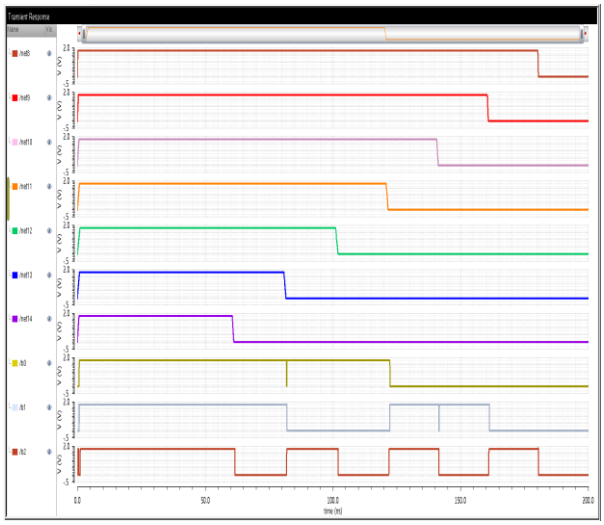

Fig.7 Transient Response of Thermometer to Binary Encoder

The output of the Thermometer to Binary Encoder is shown in Fig. 7 and for all the input combinations a desired output is obtained. When the input to the thermometer to binary encoder is 0000000, the output is 000. Similarly, when the input to the encoder is 0000001, the output is 001 and this continues until the input to the encoder is 1111111, and the output is 111.

The transient response of the compete flash ADC for a frequency of 1MHz, 3MHz, 5MHz, and 10MHz are shown in figures (8-11). For the given analog input, all the eight combinations from 000 to 111 are observed.

A. **For 1 MHz:**

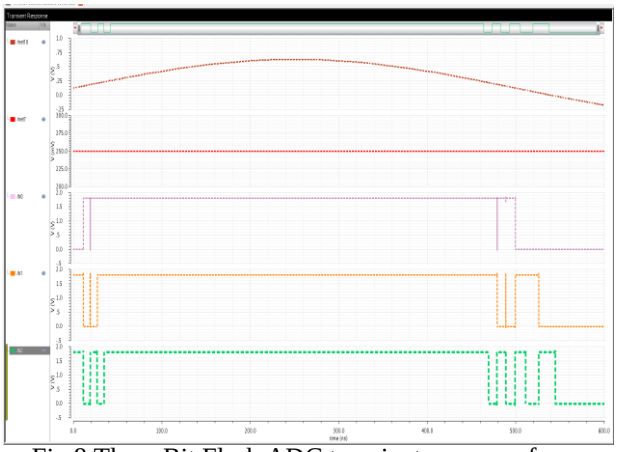

Fig.8 Three Bit Flash ADC transient response for a frequency of 1MHz

B. **For 3 MHz:**

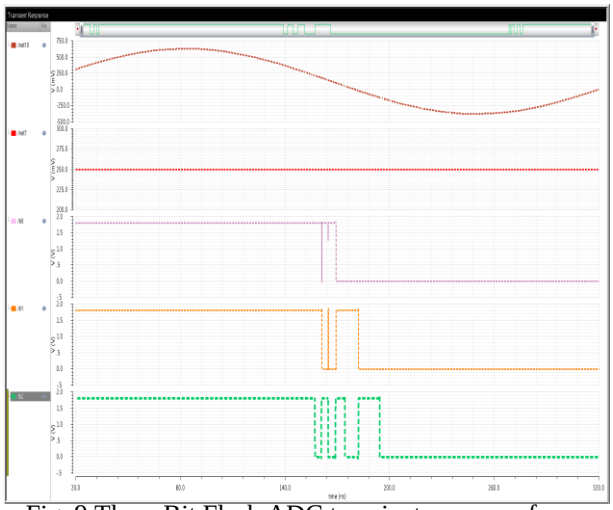

Fig. 9 Three Bit Flash ADC transient response for a frequency of 3MHz

C. **For 5 MHz:**

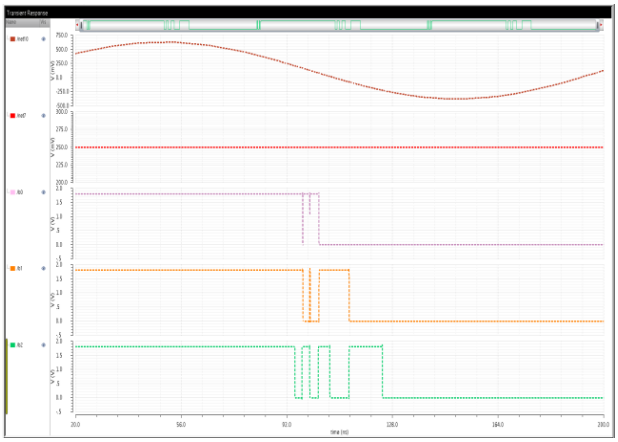

Fig.10Three Bit Flash ADC ADC transient response for a frequency of 5MHz

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D. **For 10 MHz:**

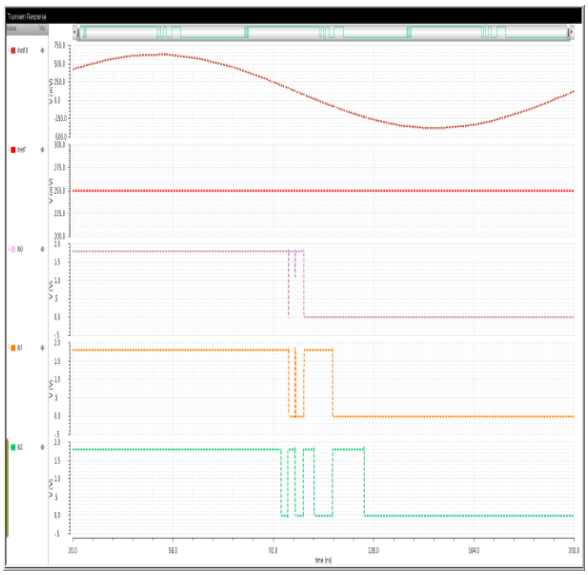

Fig. 11 Three Bit Flash ADC transient response for a frequency of 10 MHz

The transient response of the compete flash ADC for a frequency of 10MHz is shown in fig. 8. For the given analog input, all the eight combinations from 000 to 111 are observed.

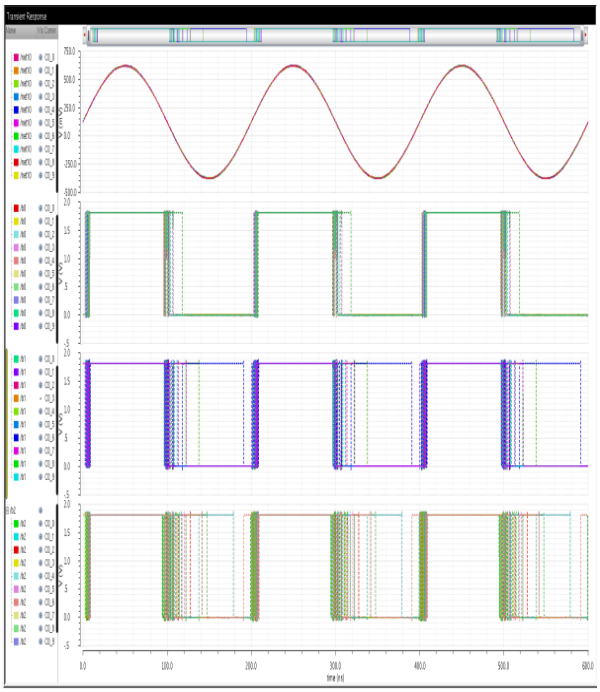

Fig.12 Corner analysis of three bit flash ADC

The corner analysis of three bit flash ADC is shown in fig. 9. For the given analog input, all the eight combinations from 000 to 111 are observed at all the corners. The response of all corners is same indicating the there is no variation in corners and hence the proposed designed meets all the specific requirements.

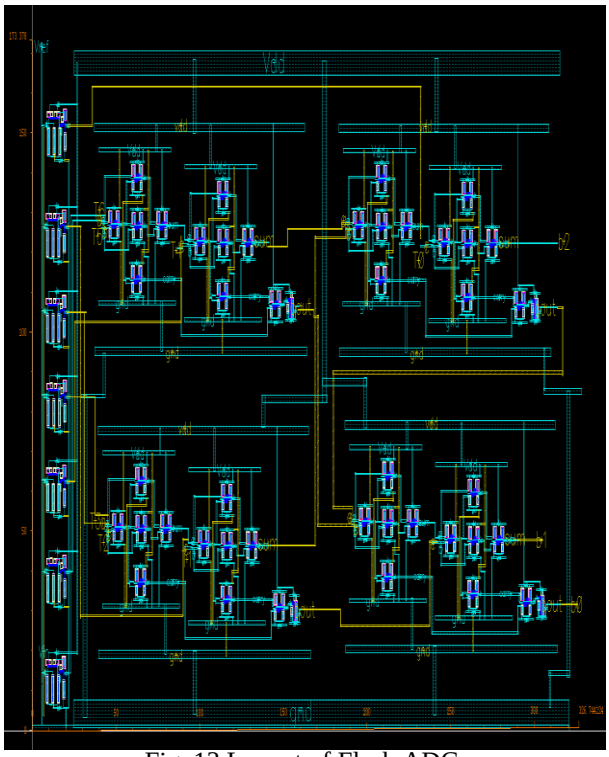

Fig. 13 Layout of Flash ADC

Area of Flash ADC = 326.7µm × 273.3 µm =0.089287 mm^2.

VI. CONCLUSION

Modern communication systems need higher information rates that have increased the demand for the high speed transceivers. For a system to workwith efficiency, all blocks of that system ought to be quick. It are often seen that the analog interfaces are main bottleneck within the whole system in terms of speed and power. This fact has emphasize researchers to develop and implement high speed analog-to- digital converters (ADCs) with low power consumption.

This paper demonstrates a high speed three bit flash ADC used for Wireless LAN applications. The designed converter is a practical approach targeted at low power high speed converter for wireless applications. This design is a flash based ADC converter with a finite output resolution of three bits and power consumption about 223uW and occupies a chip area of 0.089287 mm^2.The high speed flash ADC is being designed and verified using CADENCE Virtuoso tool with CMOS 180 nm technology.

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